**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1          1.      (Currently Amended)  A method for <u>designing a programmable logic</u>
2    <u>device</u> ~~placing circuit elements into logic blocks~~, the method comprising:
3                  assigning each of <u>a plurality of</u> ~~the~~ circuit elements to a separate abstract block,
4    wherein the circuit elements are part of a user design for a programmable integrated circuit and
5    the abstract block represents a functional attribute of its assigned circuit element;
6                  ~~grouping each~~ <u>placing a respective one or more</u> of the abstract blocks into <u>each of</u>
7    <u>a plurality of logic blocks</u> ~~a logic block~~ based at least in part on a correspondence between a
8    functional attribute of ~~the~~ <u>a particular</u> logic block and the functional attribute of ~~each~~ <u>an</u> abstract
9    block <u>placed into that logic block, wherein a first block is placed into a first logic block</u>;
10                 removing ~~a~~ <u>the</u> first ~~one of the~~ abstract <u>block</u> ~~blocks~~ from the <u>first</u> logic block in
11   response to placement information that indicates a design goal would be improved by
12   rearranging at least a portion of the user design; and
13                 placing the first abstract block into a ~~different~~ <u>second</u> logic block on the
14   programmable integrated circuit, wherein the functional attribute of ~~removed~~ <u>the first</u> abstract
15   block corresponds with a functional attribute of the ~~different~~ <u>second</u> logic block<u>, thus improving</u>
16   <u>the design goal.</u>

1          2.      (Original)  The method according to claim 1 wherein the design goal
2    includes routability and signal timing in the user design.

1          3.      (Original)  The method according to claim 1 wherein the circuit elements
2    include lookup tables and registers.

1                    4.        (Original)  The method according to claim 1 wherein the circuit elements

2        include DSP blocks and RAM blocks.

1                    5.        (Currently Amended)  The method according to claim 1 ~~further~~

2        ~~comprising:~~ wherein placing a respective one or more of the abstract blocks into each of a

3        plurality of logic blocks further comprises:

4                            determining whether placing an abstract block assigned to a particular ~~each~~ circuit

5        element into ~~the~~ a specific logic block violates any of a set of design rules relating to ~~the~~ that

6        specific logic block, wherein the logic blocks are grouped into clusters; and

7                            determining whether placing the abstract block ~~each of the circuit elements~~ into a

8        cluster containing that specific logic block violates any of a set of design rules relating to ~~the~~ that

9        cluster.

1                    6.        (Original)  The method according to claim 5 wherein each of the abstract

2        blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and

3        the attraction measures a number of nets and connections of nets absorbed into the cluster if the

4        abstract block is placed inside the cluster.

1                    7.        (Original)  The method according to claim 5 wherein each of the abstract

2        blocks are grouped into a cluster based on an attraction of the abstract block to the cluster, and

3        the attraction measures a number of timing critical connections absorbed into the cluster if the

4        abstract block is placed inside the cluster.

1                    8.        (Currently Amended)  The method according to claim 5 ~~further~~

2        ~~comprising:~~ wherein placing a respective one or more of the abstract blocks into each of a

3        plurality of logic blocks further comprises:

4                            placing ~~one of~~ the abstract block ~~blocks~~ into another logic block within the same

5        cluster if placing that abstract block into ~~the~~ that specific logic block violates any of the design

6        rules relating to ~~the~~ that specific logic block; and

Appl. No. 10/716,309
Amdt. dated March 20, 2007
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2825

PATENT

7                  placing ~~one of~~ the abstract <u>block</u> ~~blocks~~ into another cluster if placing that

8   abstract block into ~~the~~ <u>that</u> cluster violates any of the design rules relating to ~~the~~ <u>that</u> cluster.

1          9.    (Currently Amended)  The method according to claim 1 wherein the logic

2   blocks implement functions performed by two lookup tables with less than an integer k unique

3   input variables; and the method further comprises:

4                  determining whether ~~grouping each of the~~ <u>placing an</u> abstract <u>block</u> ~~blocks~~ into

5   ~~the~~ <u>a</u> logic block causes ~~any of the~~ <u>that</u> logic <u>block</u> ~~blocks~~ to have more than k unique input

6   variables.

1          10.    (Original)  The method according to claim 1 wherein the placement

2   information includes floorplanning information.

1          11.    (Original)  The method according to claim 1 wherein the placement

2   information includes partition information.

1          12.    (Previously Presented)  The method according to claim 1 wherein the

2   placement information includes data obtained by a previous placement of a portion of the user

3   design on the programmable integrated circuit.

1          13.    (Canceled)

1          14.    (Currently Amended)  A computer program product stored on a computer

2   readable medium for <u>designing</u> ~~placing circuit elements in a user design for~~ a programmable

3   integrated circuit ~~into logic blocks~~, the computer program product comprising:

4                  computer program instructions for assigning each of <u>a plurality of</u> ~~the~~ circuit

5   elements to a separate abstract block, wherein the abstract block represents a functional attribute

6   of its assigned circuit element;

7                  computer program instructions for ~~grouping each~~ <u>placing a respective one or more</u>

8   of the abstract blocks into <u>each of a plurality of logic blocks</u> ~~a logic block~~ based at least in part

9   on a correspondence between a functional attribute of ~~the~~ <u>a particular</u> logic block and the

Appl. No. 10/716,309
Amdt. dated March 20, 2007
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2825

PATENT

10    functional attribute of ~~each~~ an abstract block <u>placed into that logic block, wherein a first block is</u>
11    <u>placed into a first logic block</u>;
12          computer program instructions for determining whether placement information
13    indicates that a design goal would be improved by moving at least one of the abstract blocks into
14    a different logic block; and
15          computer program instructions for removing the ~~at least one~~ <u>first</u> abstract block
16    from a first logic block and placing the ~~at least one~~ <u>first</u> abstract block into a second logic block
17    in response to the determination based on the placement information, wherein the functional
18    attribute of the removed <u>first</u> abstract block corresponds with a functional attribute of the
19    ~~different~~ <u>second</u> logic block.

1          15.    (Original)  The computer program product as defined in claim 14 wherein
2    the design goal includes signal timing and routability in the user design.

1          16.    (Currently Amended)  The computer program product as defined in claim
2    14 wherein the logic blocks are grouped into clusters of logic blocks, and the computer program
3    instructions for ~~grouping each~~ <u>placing a respective one or more</u> of the abstract blocks into <u>each</u>
4    <u>of a plurality of logic blocks</u> ~~a logic block~~ further comprises computer program instructions for
5    grouping each of the abstract blocks into a cluster of logic blocks based on an attraction of the
6    abstract block to the cluster.

1          17.    (Currently Amended)  The computer program product as defined in claim
2    16 further comprising:
3          computer program instructions for determining whether ~~grouping~~ <u>placing</u> the
4    abstract blocks into the clusters violates any design rules of the clusters; and
5          computer program instructions for determining whether ~~grouping~~ <u>placing</u> the
6    abstract blocks into the logic blocks violates any design rules of the logic blocks.

1          18.    (Original)  The computer program product as defined in claim 14 wherein
2    some of the circuit elements are lookup tables, and some of the circuit elements are registers.

Appl. No. 10/716,309
Amdt. dated March 20, 2007
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2825

PATENT

1           19.    (Original)  The computer program product as defined in claim 16 wherein
2  the attraction measures a number of nets and connections of nets absorbed into the cluster if the
3  abstract block is placed inside the cluster.

1           20.    (Original)  The computer program product as defined in claim 16 wherein
2  the attraction measures a number of timing critical connections absorbed into the cluster if the
3  abstract block is placed inside the cluster.

1           21.    (Currently Amended)  The computer program product as defined in claim
2  17 further comprising:
3           computer program instructions for placing one of the abstract blocks into another
4  logic block if placing that abstract block to the logic block violates any of the design rules
5  relating to the logic block in which that abstract block was first placed.

1           22.    (Previously Presented)  The computer program product as defined in claim
2  17 further comprising:
3           computer program instructions for placing one of the abstract blocks to another
4  cluster if placing that abstract block to the first cluster violates any of the design rules relating to
5  the first cluster.

1           23.    (Currently Amended)  The computer program product as defined in claim
2  14 further comprising:
3           computer program instructions for determining whether placing the abstract
4  blocks to into the logic blocks causes any of the logic blocks to have more than k unique input
5  variables,
6           wherein the logic blocks are configurable to implement functions performed by
7  two lookup tables with less than k unique input variables.

1           24.    (Original)  The computer program product as defined in claim 14 wherein
2  the placement information includes floorplanning information.

Appl. No. 10/716,309
Amdt. dated March 20, 2007
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2825

PATENT

1        25.    (Original)  The computer program product as defined in claim 14 wherein

2  the placement information includes partition information.

1        26.    (Original)  The computer program product as defined in claim 14 wherein

2  the placement information includes data obtained by placing logic blocks that implement

3  portions of the user design on the programmable integrated circuit.

1        27.    (Currently Amended)  The method of claim 1, wherein ~~the~~ each logic

2  block includes a first functional attribute and a second functional attribute, and wherein ~~grouping~~

3  placing each of the abstract blocks into a logic block further comprises:

4        assigning ~~a~~ the first abstract block associated with a first circuit element to the

5  first functional attribute of the first logic block; and

6        assigning a second abstract block associated with a second circuit element to the

7  second functional attribute of the first logic block, such that the first logic block is assigned the

8  functional attributes of the first and second circuit elements.

1        28.    (Previously Presented)  The method of claim 27, wherein the first

2  functional attribute of the logic block includes a register and the functional attribute of the first

3  circuit element includes a register.

1        29.    (Previously Presented)  The method of claim 27, wherein the second

2  functional attribute of the logic block includes a look-up table circuit adapted to implement a

3  logic function and the functional attribute of the first circuit element includes a logic function

4  capable of being implemented by the look-up table circuit.

1        29.    (New)  The method of claim 1 wherein a second abstract block is placed

2  into the first logic block prior to removing the first abstract block.